APPLICATION NOTE

(DOC No. HX8218-A-AN)

HX8218-A

960CH TFT LCD Source Driver
with Built-in T-CON

Preliminary version 02 July, 2005

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http://www.himax.com.tw

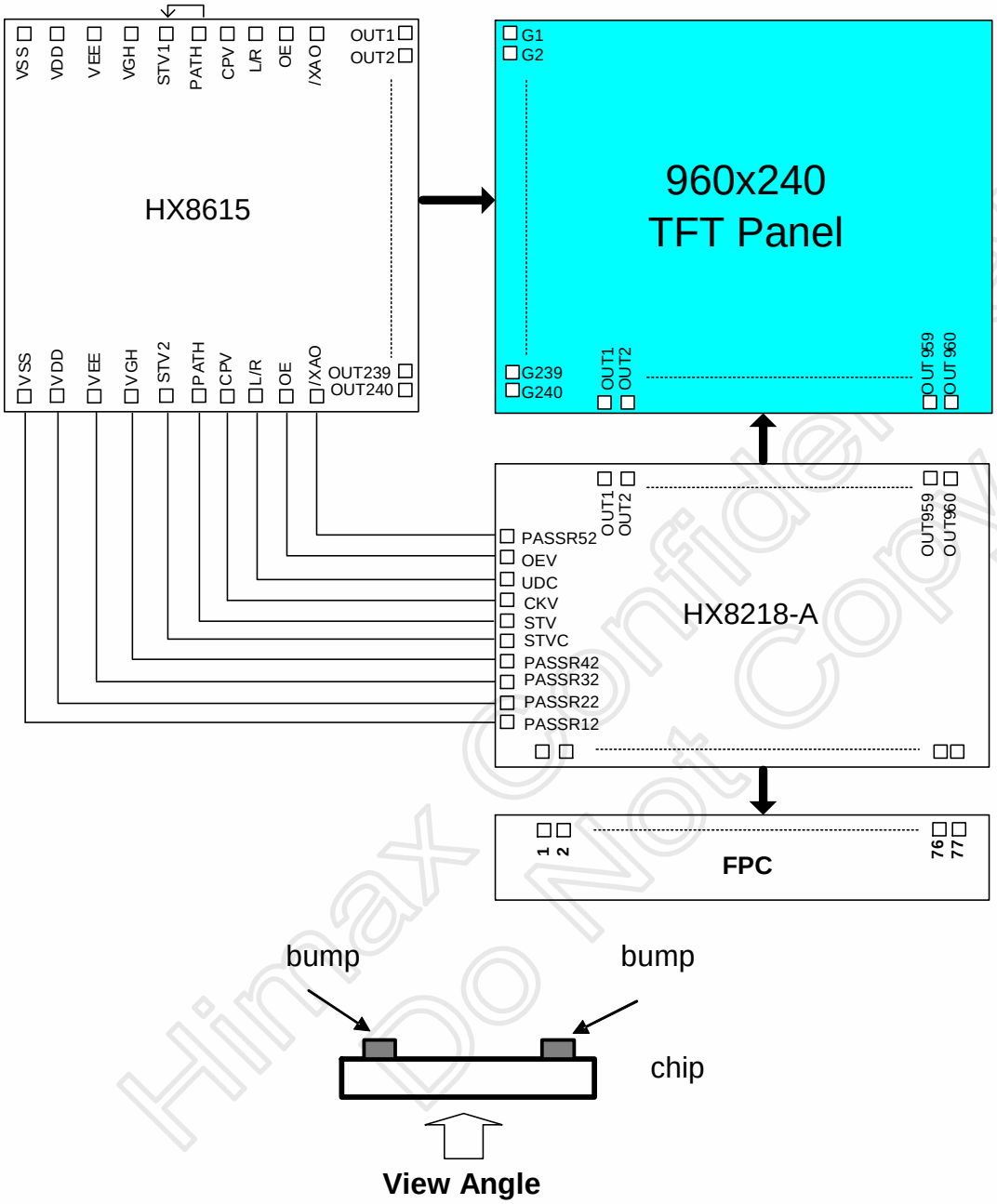
1. General Description

HX8218-A is a 960-channel output Source Driver with built-in TCON and DAC. The interface follows digital 8-bits serial/24-bits parallel RGB, or CCIR601/656 input signals and digital control timing signals. The DAC supports transferring digital RGB data to analog RGB data for the internal Source Driver. The TCON generates the 960x240 resolution timing to Source driver and Gate Driver.

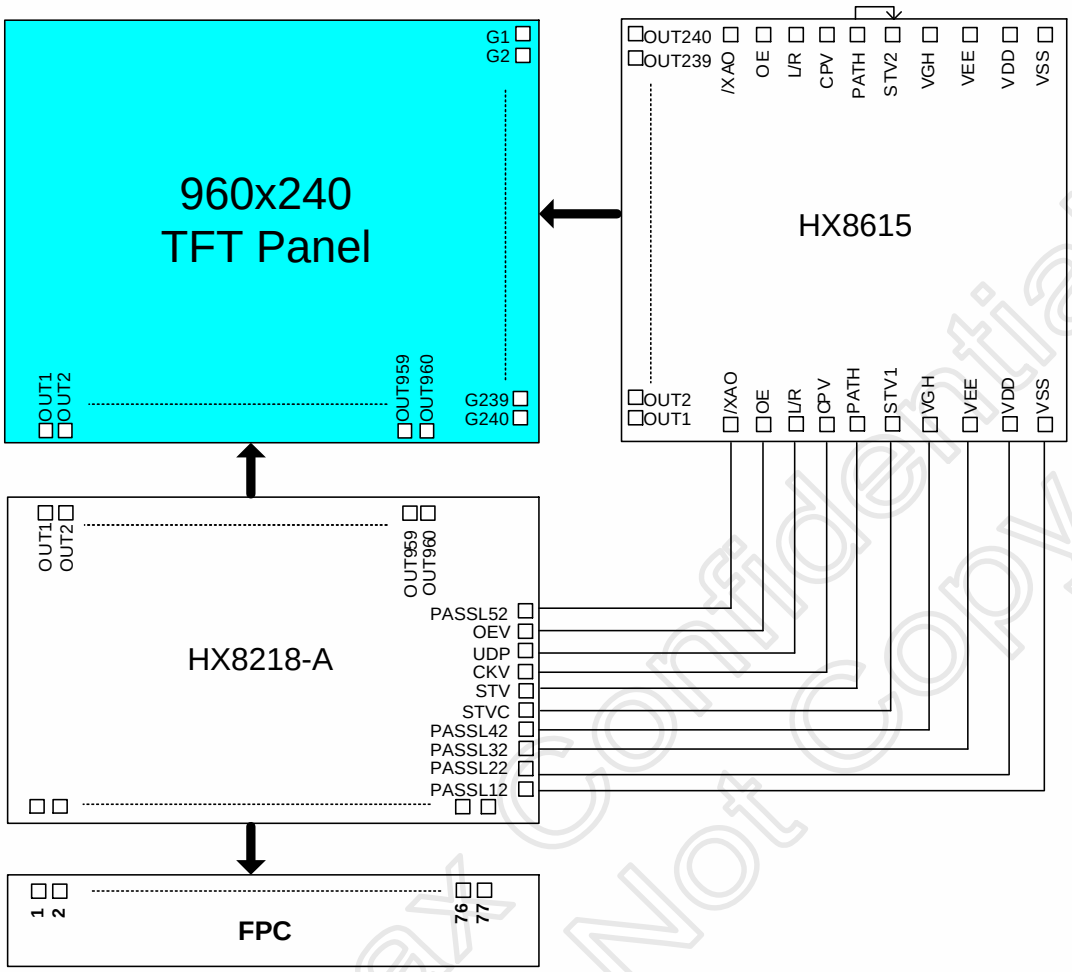
The Source Driver implements 2 lines of sample and hold circuits. While sampling video signals, the previously sampled data can be output synchronously through driver output channels. And simultaneous or sequential sampling can be chosen for matching the pixel array type.

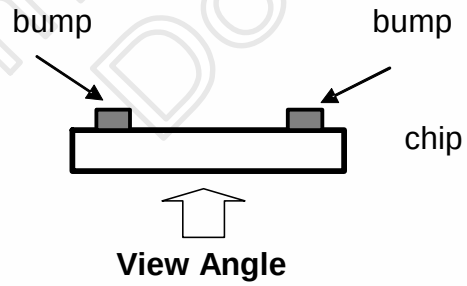
The timing controller provides horizontal and vertical control timing to source and gate drivers. With built-in DAC and operational amplifiers, the gamma correction can be performed and digital data is converted to analog signal and sends to source driver.

2. On Panel Connection (L)

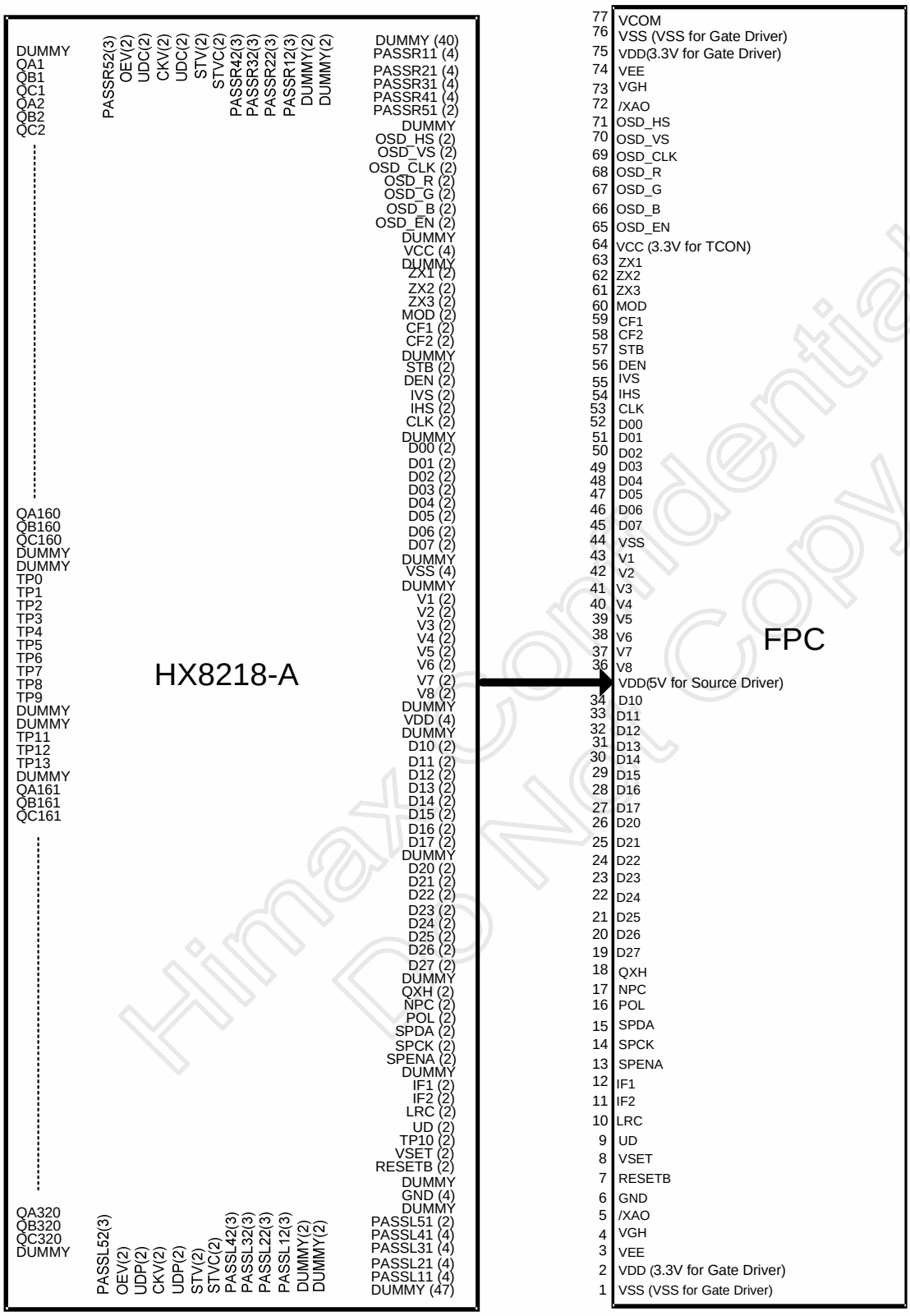


3. On Panel Connection (R)





4. FPC



5. Pin in FPC

5.1 Input Data Mode in FPC

	D00 ~ D07	D10 ~ D17	D20 ~ D27
Serial RGB	V	X	X
Parallel RGB	V	V	V
CCIR 656	V	X	X
CCIR 601	V	X	X

5.2 Input Data Format Setting

IF2	IF1	Input data format
L	L	Serial RGB (default)
L	H	Parallel RGB
H	L	CCIR601
H	H	CCIR656

5.3 Description in FPC

5.3.1

OSD : If you don't want to use OSD, you just set the OSD_EN to low and others(OSD_HS, OSD_VS, OSD_CLK, OSD_R, OSD_G, OSD_B) are floating.

5.3.2

SPI : If you don't want to use SPI, you just set the SPENA to high and others(SPDA, SPCK) are floating.

5.3.3

Gamma Voltage : Set VSET to low to use the default voltage and others(V1 ~ V8) are floating and be careful to drive the V1 ~ V8, it will influence the Gamma Voltage whatever VSET set to low.

5.3.4

Color Filter : When MOD="L", delta type and others(CF1, CF2) are floating, When MOD="H", stripe type.

5.3.5

Input data sequence and color filter type

- CF1 defines the input data sequence in serial digital RGB mode as following tables.

1. CF1="L"

Scan direction	UD	Low	Low	High	High
Shift direction	LRC	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	BRG	GRB
	Even line	BRG	GRB	RGB	BGR

2. CF1="H"

Scan direction	UD	Low	Low	High	High
Shift direction	LRC	High	Low	High	Low
Data sequence	Odd line	RGB	BGR	GBR	RBG
	Even line	GBR	RBG	RGB	BGR

- For the color filter type, set MOD="H" for stripe type and the CF1&CF2 definition will have no meaning. Set MOD="L" for delta color filter and CF2 defines which kind of delta type color filter is used.

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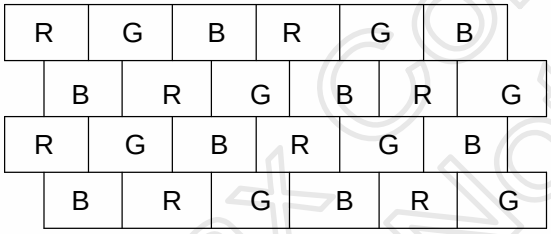
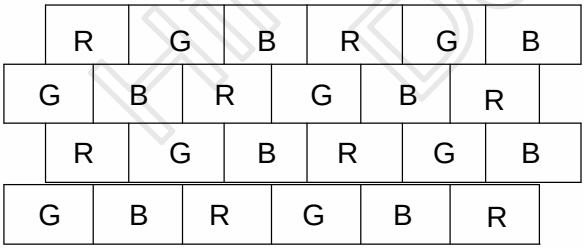
1. CF2="L", delta type 1



2. CF2="H", delta type 2:



5.3.6

Zoom Mode : The zoom in/out function is only supported in CCIR601/656 input mode in Strip type.

5.3.7

Hardware Global Reset : Low active. Normally pull high.

5.3.8

VCOM : VCOM and POL are inphase.

6. Power ON/OFF sequence

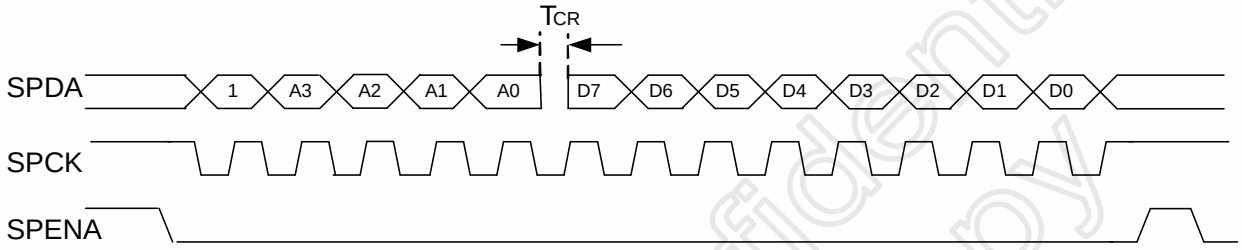
To prevent the device from damage due to latch-up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC, GND → VDD, VSS → V1~V8
Power OFF: V1~V8 → VDD, VSS → VCC, GND

7. SPI

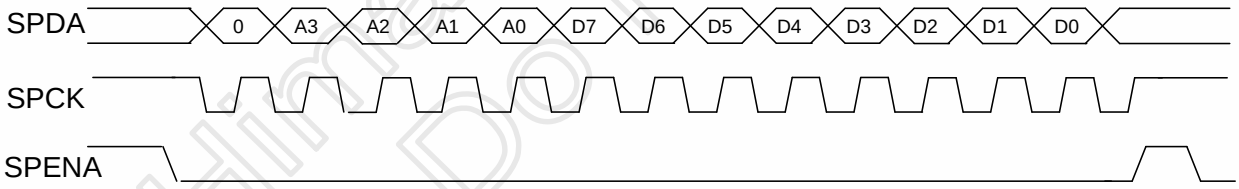
7.1 Description

- **SPI "read" timing**



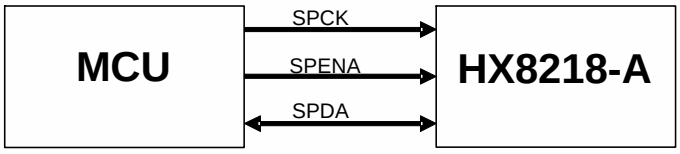
(1) Make a clock (2 MHZ) for SPCK.
(2) Set SPENA low to let the SPI valid.
(3) Send "1" in the MSB to show reading the SPI and the address 4-bits (A3 : MSB, A0 : LSB) in the rising edge of the SPCK then wait a half of the SPCK to read the data(D7 : MSB, D0 : LSB) in the falling edge of the SPCK.

- **SPI "write" timing**



(1) Make a clock (2 MHZ) for SPCK.
(2) Set SPENA low to let the SPI valid.
(3) Send "0" in the MSB to show writing the SPI and the address 4-bits (A3 : MSB, A0 : LSB) in the rising edge of the SPCK then read the data(D7 : MSB, D0 : LSB) in the rising edge of the SPCK.

7.2 Follow



8. System Block Diagram